# Practical Parallelism

## Tales from the trenches of commercial place and route tools

Adrian Ludwin, Altera Corp.

ParCAD @ ICCAD 2010

San Jose, November 11, 2010

*Additional information in PowerPoint speaker's notes*

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# Purpose of today's talk

- Warn you about problems we encountered
- Encourage researchers to study certain topics
- Suggest ideas for tool vendors

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# About myself

- Software engineer on Quartus II
  – Altera's CAD suite for FPGA design
- Worked on several parallel algorithms in QII
  – Either developed them myself or assisted other engineers
- The hardest algorithm was parallel placement
  – A Ludwin, V Betz and K Padalia: "High-quality, deterministic parallel placement for FPGAs on commodity hardware," FPGA 2008

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# Why Altera is investing in parallelism

***Here's that slide again!***

Logic Elements (Thousands)

900
800
700
600
500
400
300
200
100
0

Logic Elements
Relative CPU Speed

Relative SpecINT

90
80
70
60
50
40
30
20
10
0

1998 2000 2002 2004 2006 2008 2010

Year Introduced

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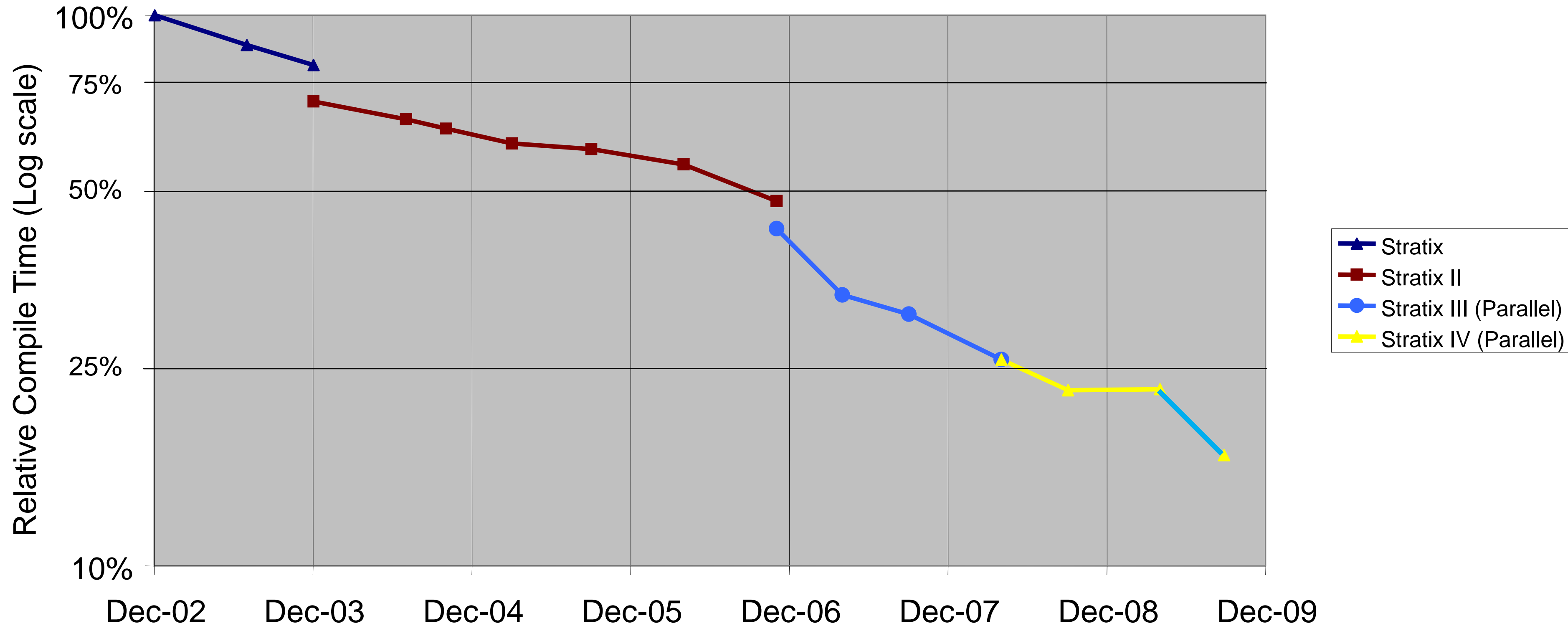
# Quartus II compile time history

## *Fixed design on a fixed CPU*




## *Not shown: savings from hierarchical/incremental design*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# Agenda: three types of challenges

- Development
- Determinism
- Quality

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# Development challenges

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# Who’s embarrassed?

- QII has few “embarrassingly parallel” algorithms
- Many algorithms have thousands of lines of code
- Fitter (“P+R”) has many distinct algorithms
  - Periphery placement (eg PLLs, transceivers, clocks)
  - Register packing
  - Assorted netlist transformations
  - Clustering
  - Placement
  - Congestion analysis
  - Slack allocation
  - Routing
  - Timing analysis
  - High-speed/low-power tile setting
  - Beneficial skew

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# Fitter: no one major runtime hog!

Algorithm 7 3%

Algorithm 6 5%

Algorithm 5 6%

Algorithm 4 9%

Algorithm 3 10%

Timing analysis 14%

Place and route 24%

Other + disk IO 29%

*One Stratix V design, internal 10.1 build. Total Fitter time: about three hours*

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# Development challenges

Part 1 of 3: ensuring thread safety

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# About Quartus II code

- Mainly C/C++
- Most algorithms have similar template:
  - Initialize permanent data structures
  - Initialize temporary ("scratch space") data structures
  - Do work
  - Remove data structures

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# That's easy!

- Simple to make thread-safe, in theory
- Just find all global variables (in C):
  - Permanent data: lock or make per-thread copies
  - Scratch space data: make per-thread
  - Only care about data that's *written*, not read-only
- Harder in C++ but similar idea
- Problem: hard to find suitable tools

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# Tools to find possible data races

- Existing tools are overkill for our simple problem
- Intel Parallel Advisor?
  - Didn't exist until recently
  - 40x runtime
  - 12x memory
  - Requires testcases
  - Emits message for every *error* instead of every *variable*
- Coverity?
  - Harder to run
  - Expensive (if you don't already have it)
  - Also emits messages for errors instead of variables

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# So we wrote our own

- GCC backend, Perl/Tk front-end
  - GCC finds functions, globals
  - Post-processor reads GCC output
  - Also maintain list of “known good” functions/globals
- We called it “Deep Code Inspection”
- Anyone want to develop it for us?

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# Development challenges

Part 2 of 3: writing the algorithm

*Covered in the rest of this presentation*

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# Development challenges

Part 3 of 3: quality assurance

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# Testing issues

- Runtime
- Stability
- Determinism

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# Testing runtime

## *Options on a twelve-core box*

**Run 1 instance of QII**

- Very poor throughput
- Near-perfect runtime measurements

**Run 12 instances of QII**

- Good throughput
- Noisy, low-fidelity runtime measurements

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# Testing stability

- Now, we use standard tools
  - Coverity, Thread Checker, helgrind
  - Push runtime tools to/over to the limit
- We allow “unsafe” operations by design
  - Our algorithms are allowed to detect these and recover
  - But the tools have no way of knowing this
  - No good way to separate “false” positives from real mistakes
- We rely heavily on our own stability testing

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# Testing determinism

- Compare final output of multiple runs
- Use “cookies” to further ensure determinism
  - Can’t just look at the final result
  - What if we chose *not* to do something?
  - Did we make that decision deterministically?
- Difficult to choose good testcases
  - Running them all multiple times would take thousands of hours

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# Development challenges summary

- Thread safety is hard, but tools could help
- Testing is hard, and we just have to live with it

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# Ensuring determinism

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# Is this really important?

- Rarely studied in academic literature
  - Eg: of the ~10 papers I cited, only two were deterministic, and one of them didn't even bother to mention it
- But we think it's essential
  - Both for the vendor and the customer

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# Motivation for vendors: quality

- Deterministic tools are easier to verify
  - Especially given our difficulty with tools
  - Testing for determinism achieves similar goal
- Reproducing bugs from customers

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# Motivations for customers

- Customers do re-run unmodified designs
  - Not good if the result changes randomly
  - Altera sometimes has to re-run their designs as well
- Some customers *require* determinism (military)
  - Concerned about software being compromised
  - Need to compare output to a “known good” version
  - If output changes randomly, this is not possible

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# Challenges achieving determinism

- Algorithmic development
- Algorithmic performance
- Hardware limitations

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# Challenge: algorithmic development

- First approach: strictly partition the problem
  - *Guarantee* no interactions between cores
- Second approach: track and resolve interactions
  - Compatible with a partial partitioning
  - Are you *sure* you've actually tracked/resolved everything?
  - Building an algorithm to resolve interactions can be difficult

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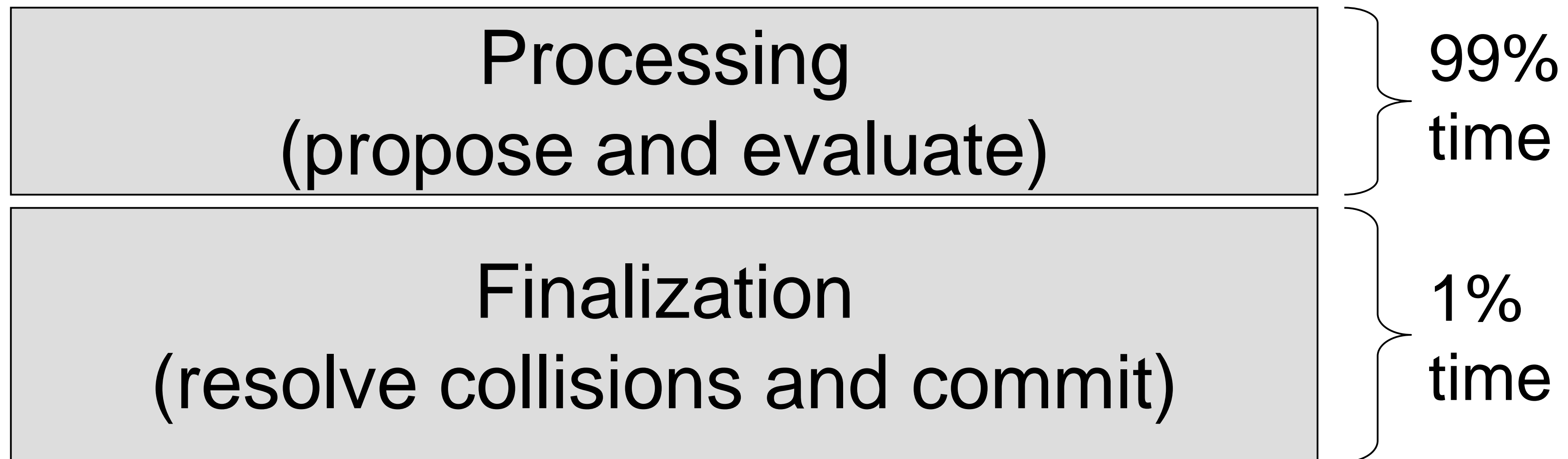
# Building a deterministic placer




This is the inner loop of the Quartus II placement algorithm. We divide it into two stages: “processing” and “finalization.” The “processing” stage is the one that is parallelized.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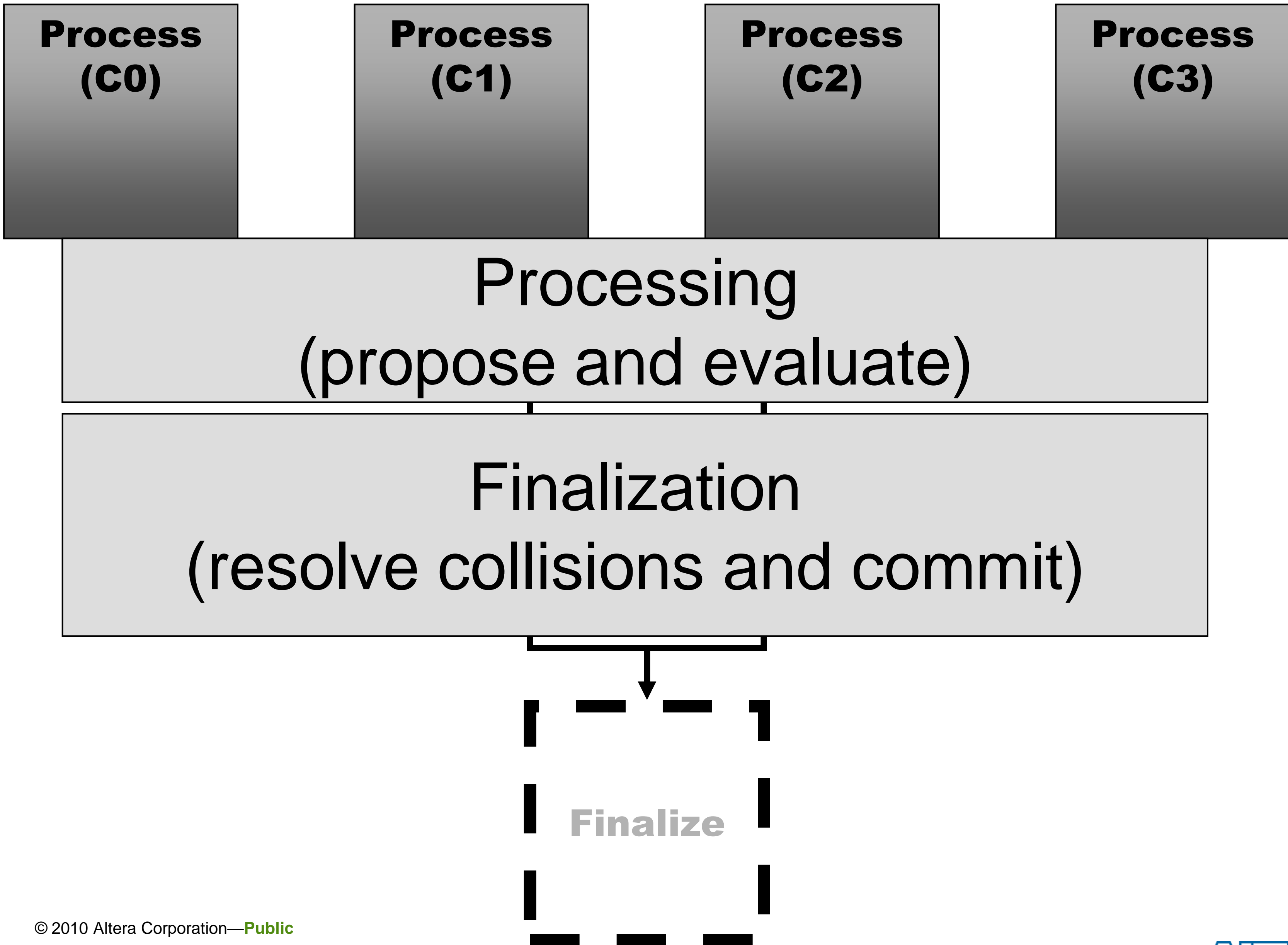


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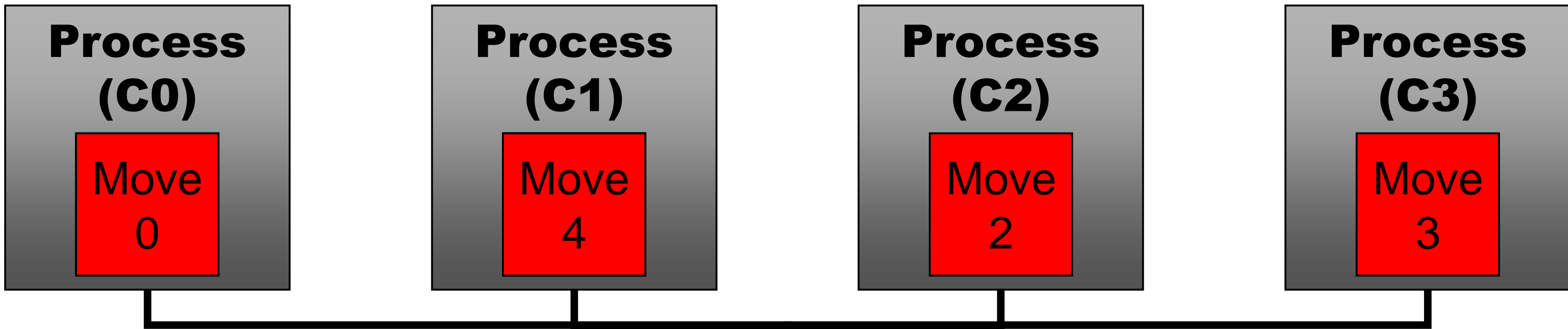


ore that processed this last move ecomes responsible for finalizing moves in the queue. Note that it t have to wait for any other core; ws that the move it inserted went to the front of the queue.

inishes out of order, it sits in the y queue until the earlier moves ished. Meanwhile, the core that sed it goes onto the next move. s not stall and wait for any other cores.

All four cores begin processing moves at the same time. Since finalizing moves is so fast, it would be a waste to devote a core to that task. Instead, all cores have the ability to finalize moves at the appropriate time, as this example will show.

The priority queue now has two moves ready to be finalized.

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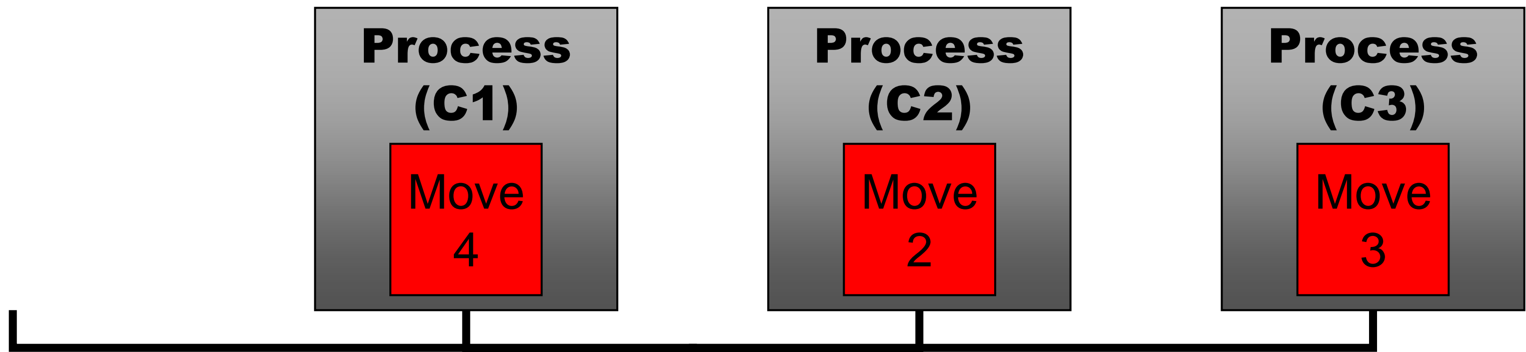
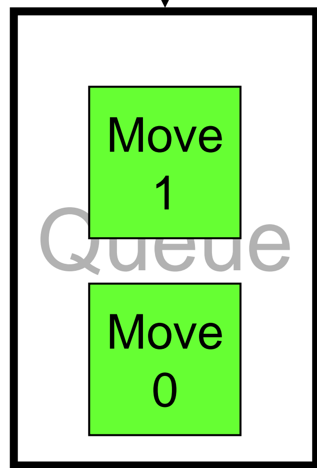
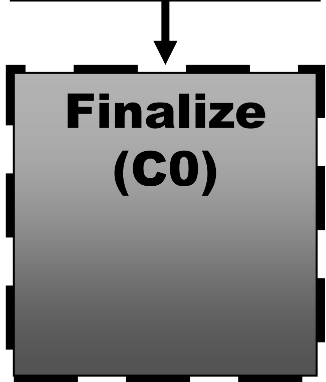



The core that processed this last move now becomes responsible for finalizing all the moves in the queue. Note that it did not have to wait for any other core; it knows that the move it inserted went to the front of the queue.




Finalization is where all interactions between moves (aka collisions) are resolved.

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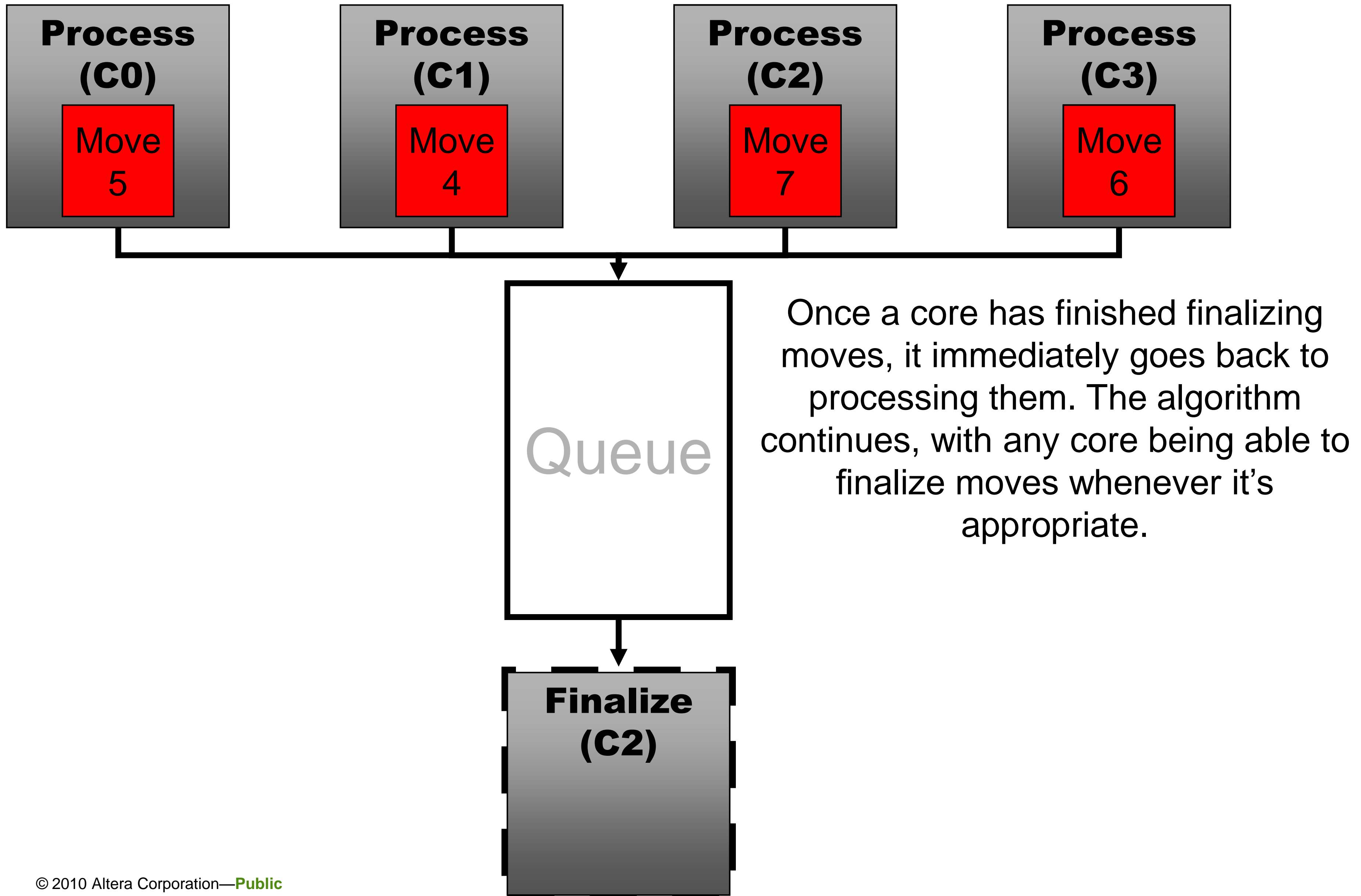


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# Challenge: algorithm performance

- Partitioning often costs runtime or quality
  - Quality: cross-partition modifications forbidden or discouraged
  - Runtime: maybe every partition didn't need same optimization
- Tracking/resolving costs runtime
  - Both tracking and resolving incur direct overhead

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# Challenge: hardware limitations

- Determinism implies intra-core communication
- Intra-core communication is slow
  - Limited bandwidth between cores
  - Commonly-used data is not in your cache
- More fundamentally: hard to distribute

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# Possible solutions

- No silver bullet, of course
- Hardware transactional memory: bronze bullet?
  - Pros: moves much of the overhead to hardware
  - Cons: doesn't actually exist for the foreseeable future

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# Determinism summary

- We think it's vital
- It's hard to develop
- It has performance implications

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# Parallel Quality

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# We all know the runtime-quality tradeoff…

runtime

quality

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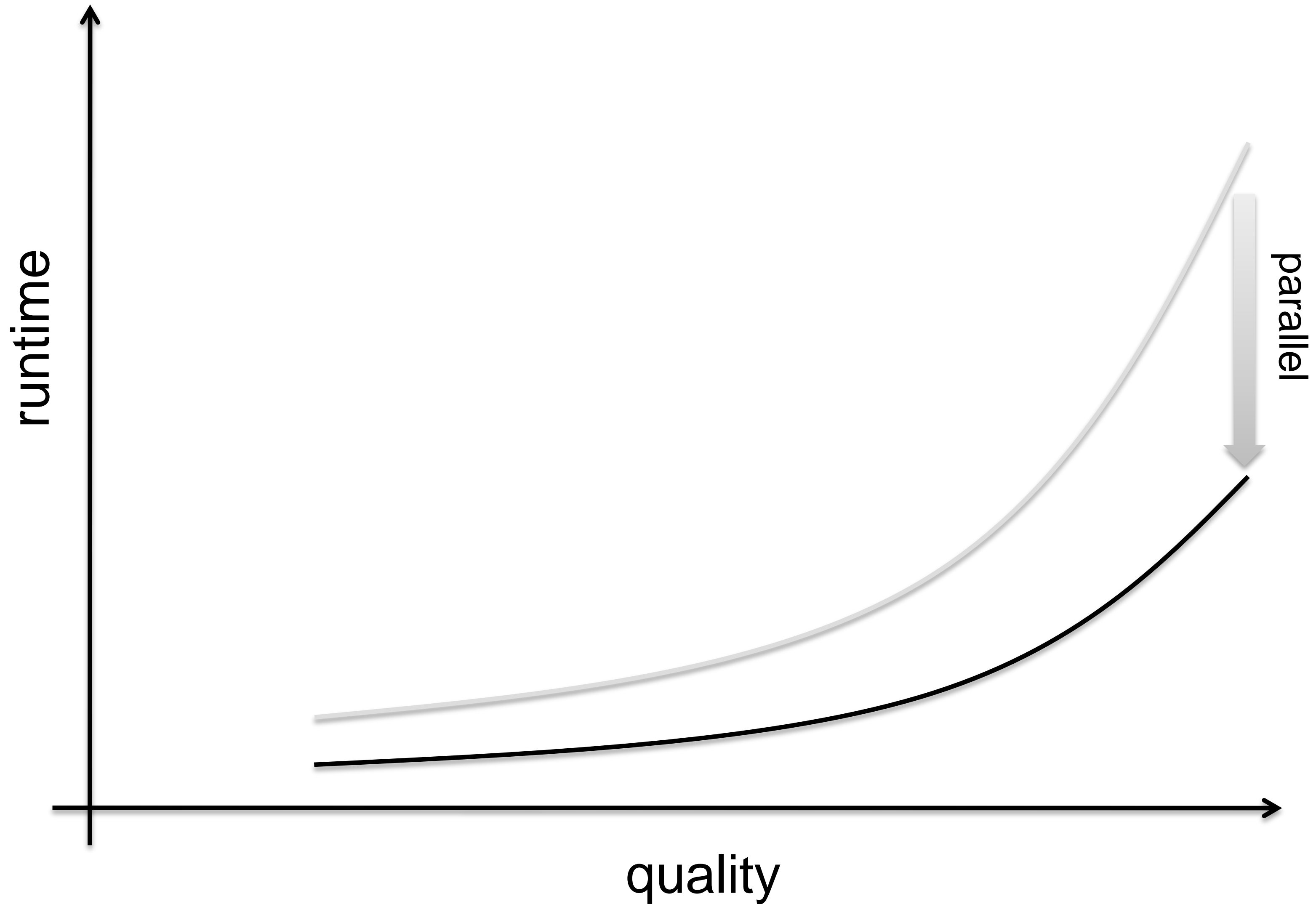
# … and this is what we want:

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# Unfortunately, it's not that simple

- Parallel likes lots of cleanly divided subtasks
  - Traditional "fast" algorithms didn't really care
- But many CAD algorithms hate partitioning
  - Can reduce both quality and runtime
- Other simplifications can have the same effect

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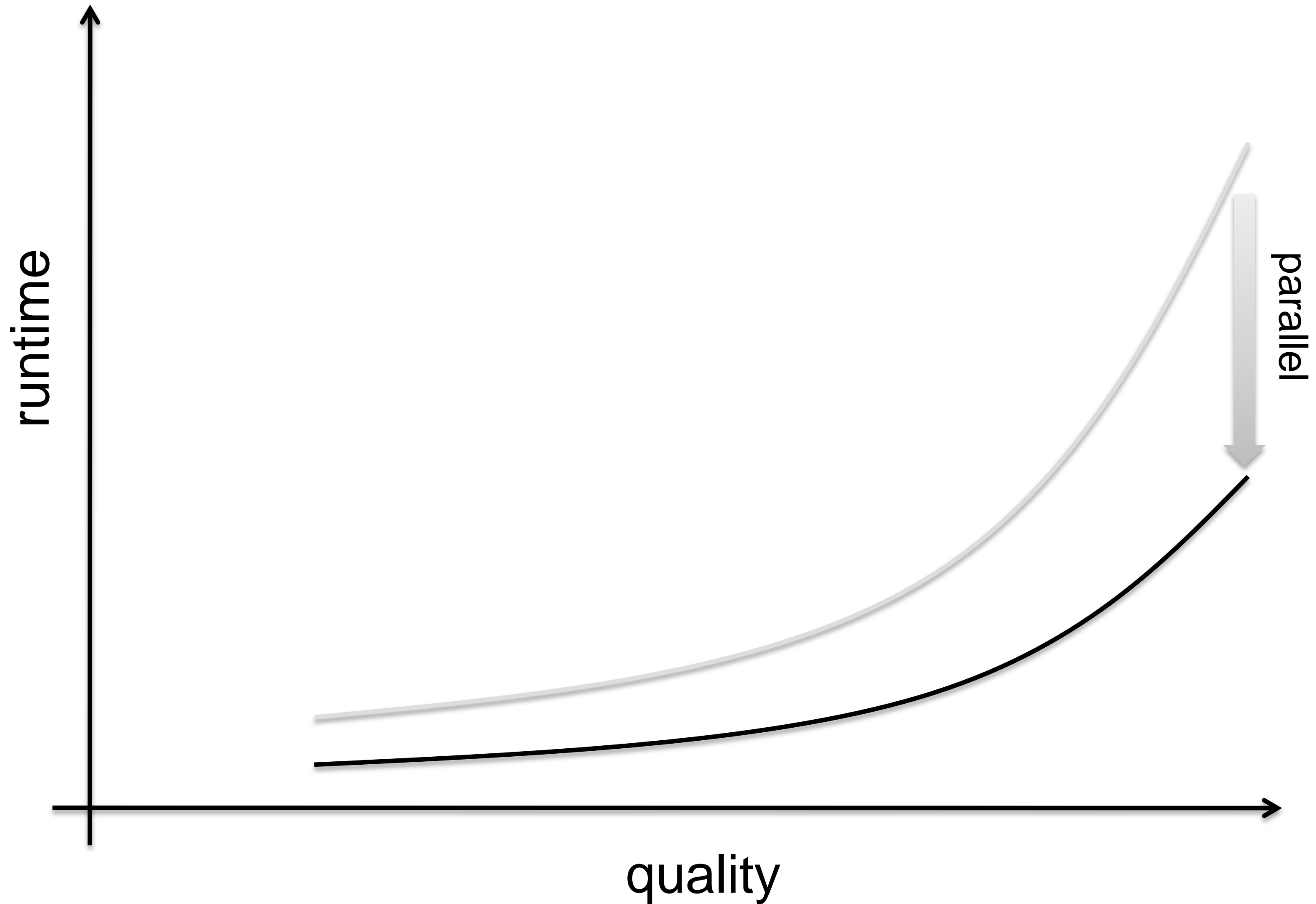
# So instead of this…

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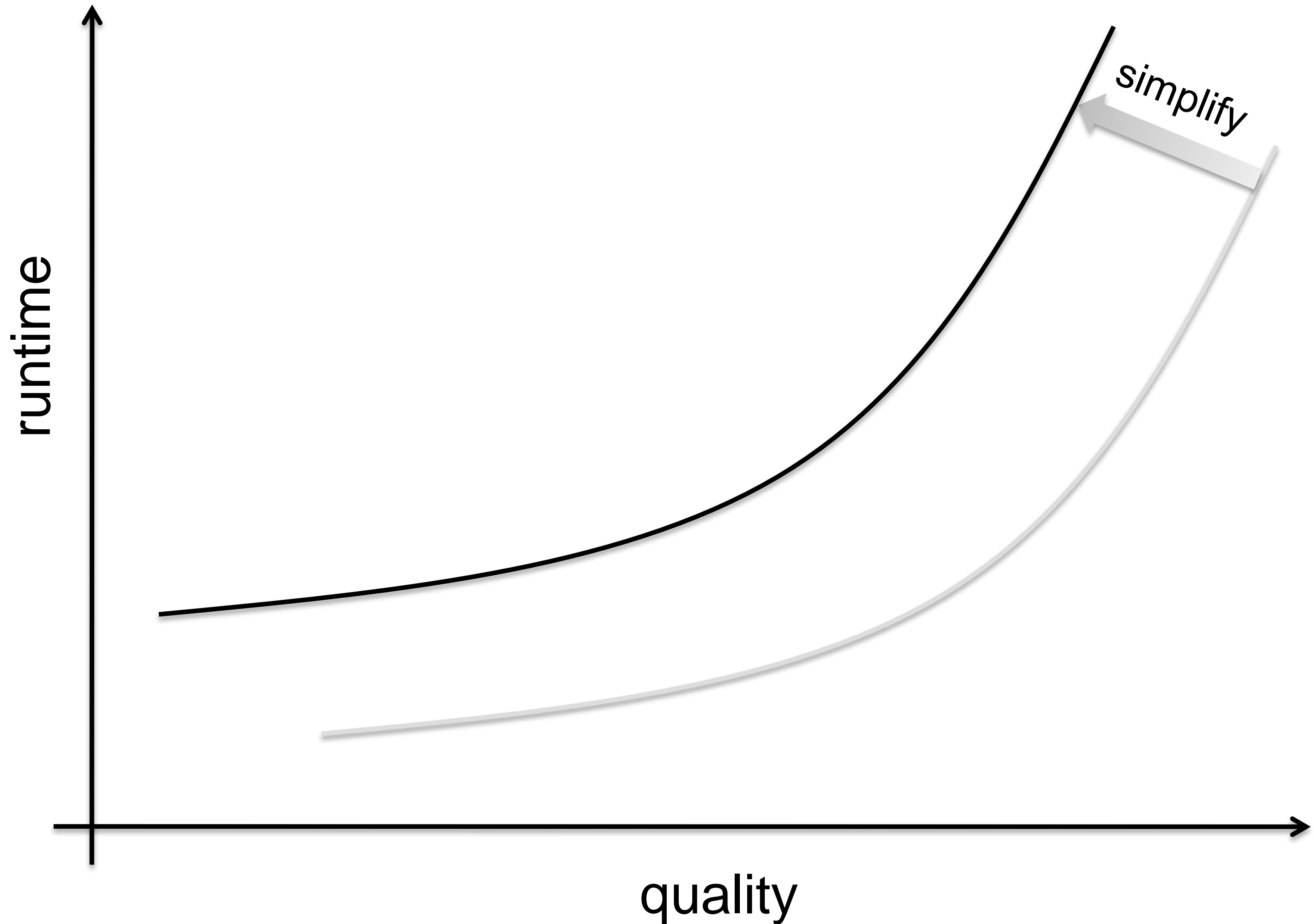
# … we "simplify" the algorithm to this …

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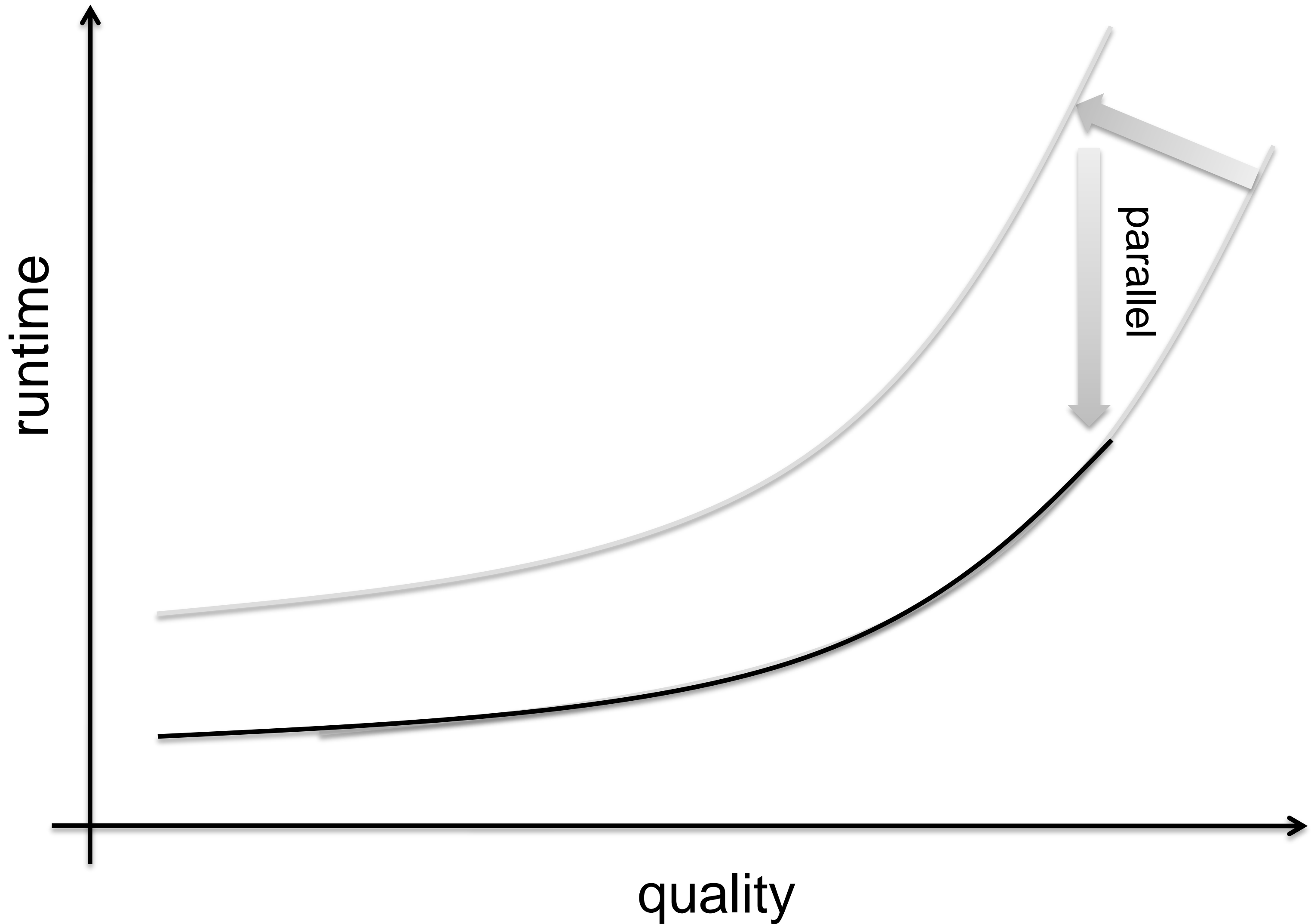
# … well that was fun, wasn't it?

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# This is sometimes easy to miss

- Parallel algorithm: “2x faster, for 10% more wire”
  - Please note that the example that follows is an exaggeration

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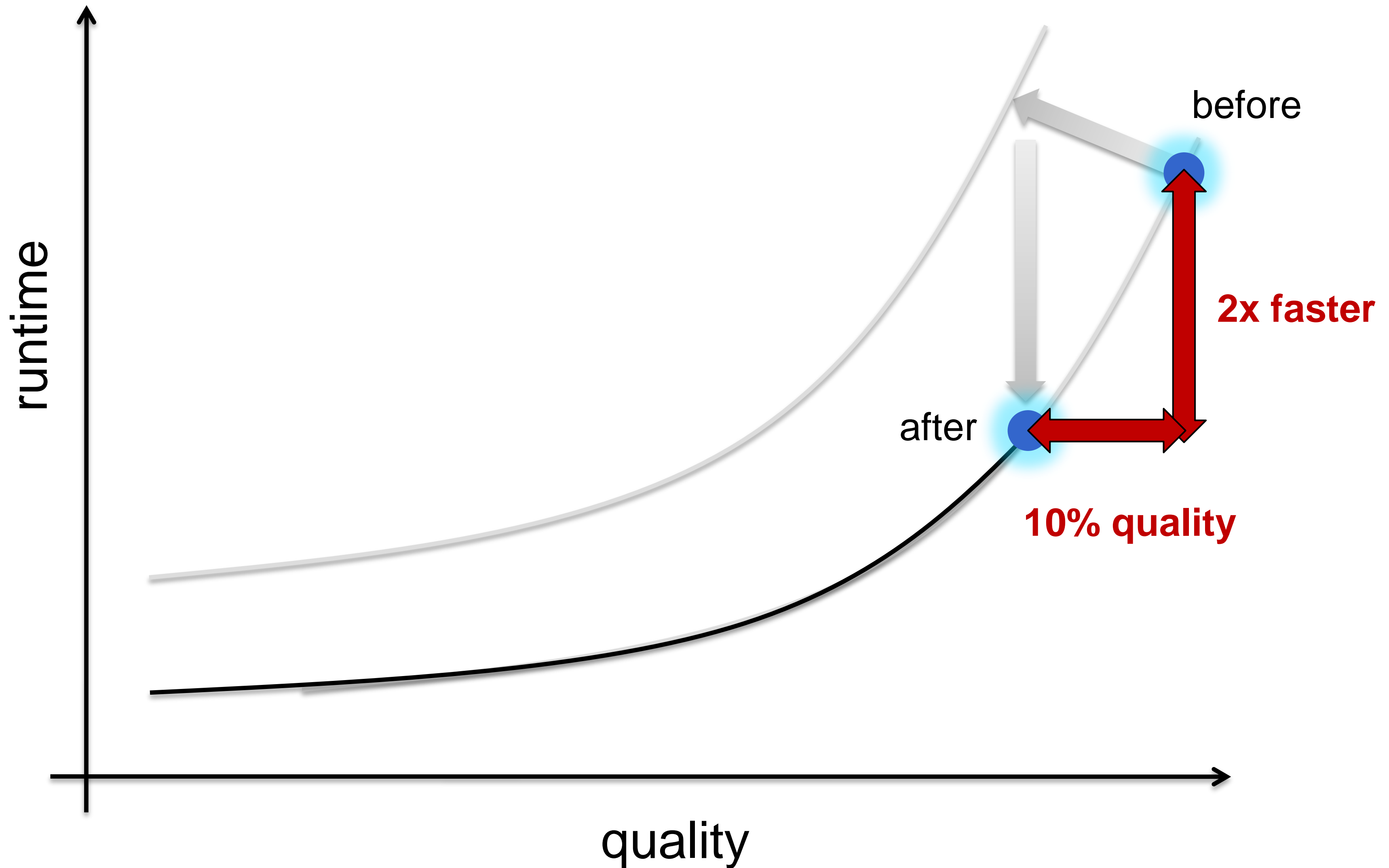
# This is sometimes easy to miss





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# What are the alternative algorithms?

- What if you only consider the simpler algorithm?
  - You might achieve a complex algorithm's runtime/quality curve
  - So it's important to know the alternative algorithms
- Could be better to accept a lower speedup
  - Obviously this depends on how much speedup is on the table

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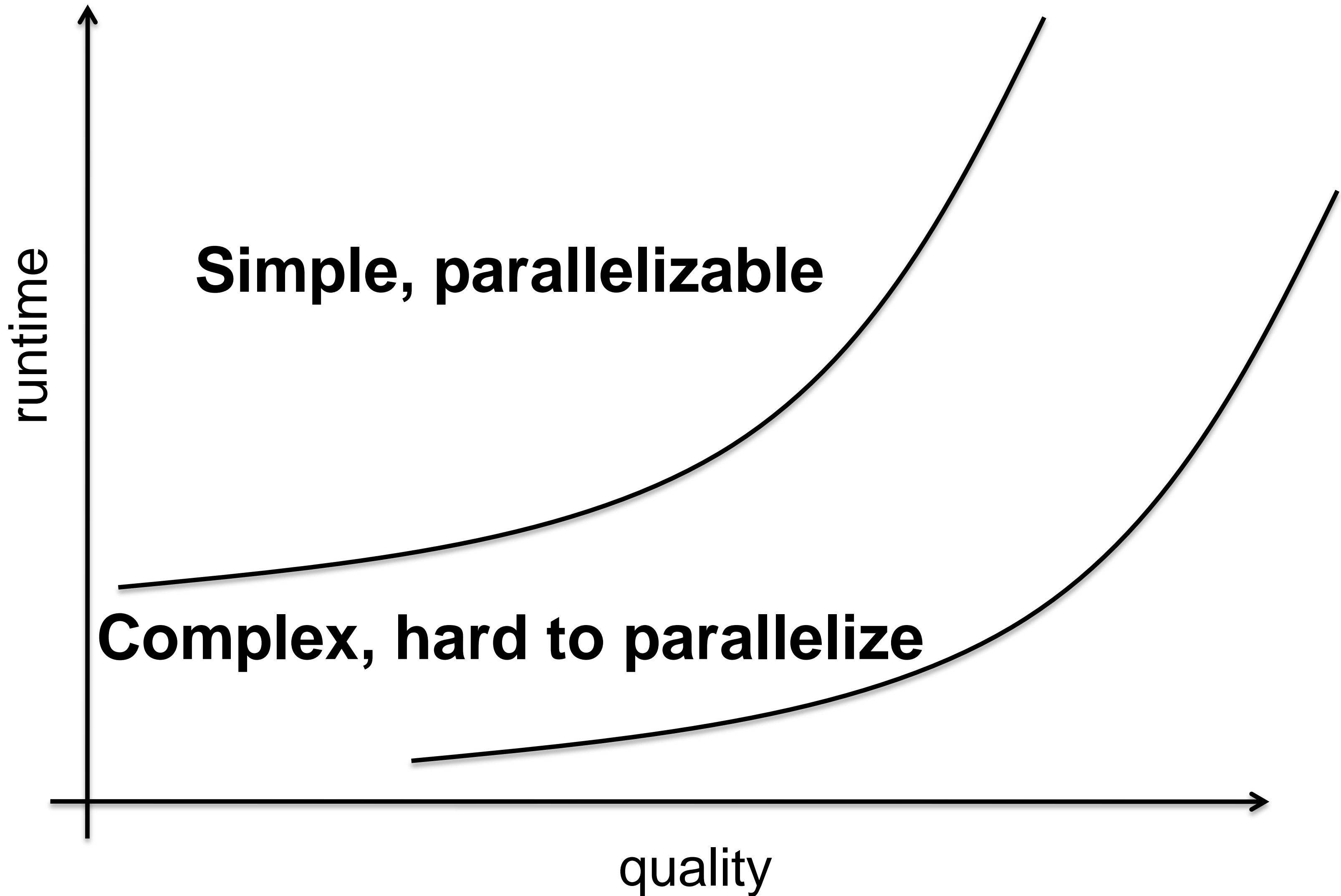
# Lower speedups are sometimes better





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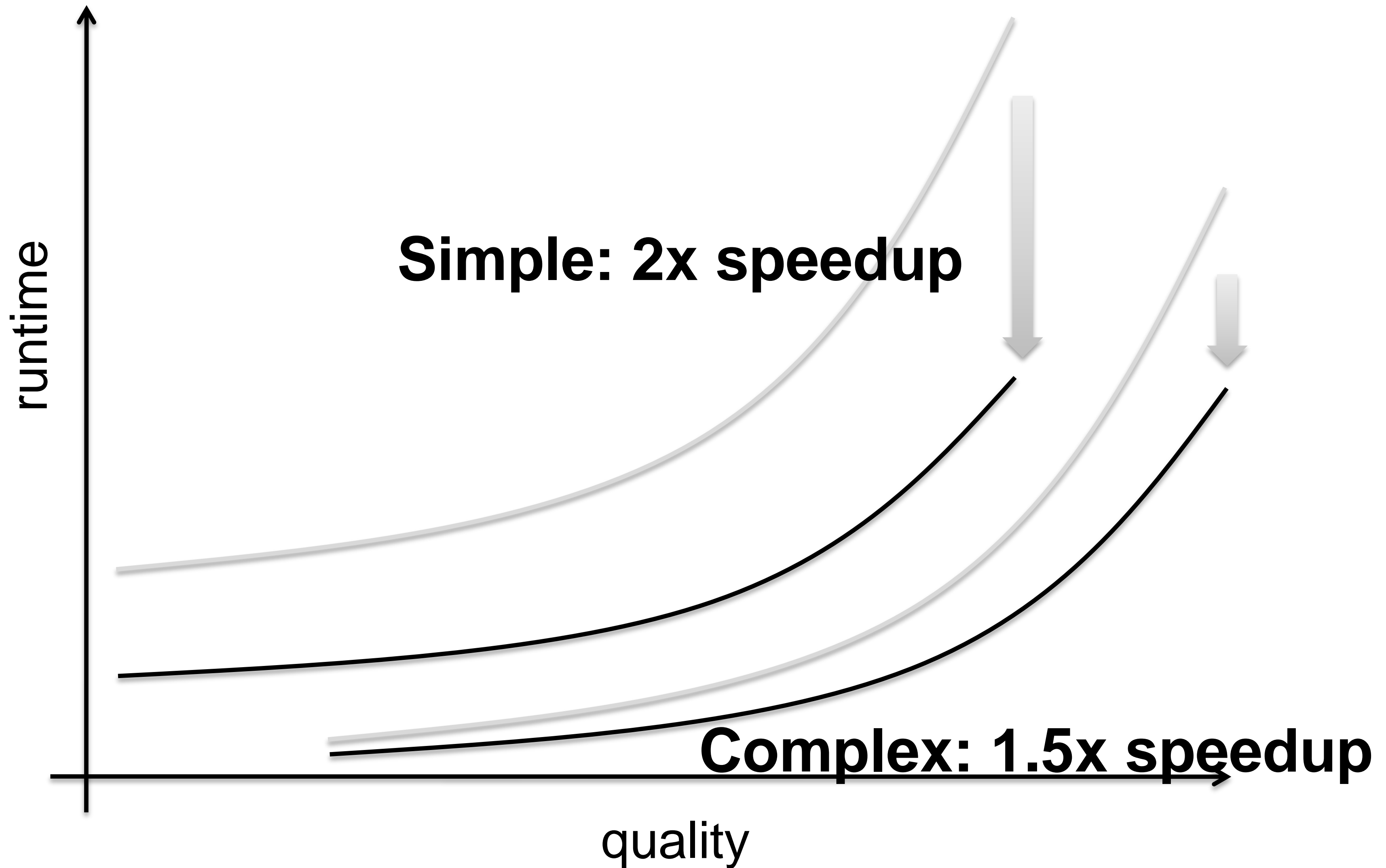


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# Concrete example: simulated annealing

- Inner loop: propose move and evaluate cost
  - A cell and proposed new location is selected at random
  - Proposed location is generally close to present location
  - Costs are generally local: eg, nets connected to the cell
- This is *relatively* easy to parallelize
  - Uniform spatial distribution of work with good spatial locality
  - Easy to partition
  - Eg Sun + Sechen '97: near-linear speedup on 6 machine cluster
    - No increase in wirelength
- Example: VPR placement algorithm
  - An academic FPGA place-and-route package

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# Complication: Quartus II placement

- Based on VPR placement algorithm
- Many important improvements over VPR
  - Neither cells nor locations selected at random (“focused moves”)
  - Proposed locations may be distant from current location
  - Many costs are less local: eg, path-based timing, clock regions
- Less spatial locality - harder to parallelize
  - 2.4x average speedup on 8 cores during the anneal (up to 3.7x)
  - 4.0x average speedup on 8 cores during the quench (up to 5.6x)

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# Comparison: VPR vs Quartus II

- At default optimization levels[1]:
  - 15% faster routed critical path, 7% lower routed wireuse
  - 35% lower placement time
- VPR can't match QII's quality for any runtime
  - Eg increased VPR runtime by 10x: still 12% worse critical path
- A parallelization of VPR that doesn't work on QII is of little use to customers who need advanced timing closure

*If you're wondering why we use simulated annealing at all, ask me after the talk…*

[1]Based on internal testing. Quartus II is very difficult to compare fairly to academic tools.

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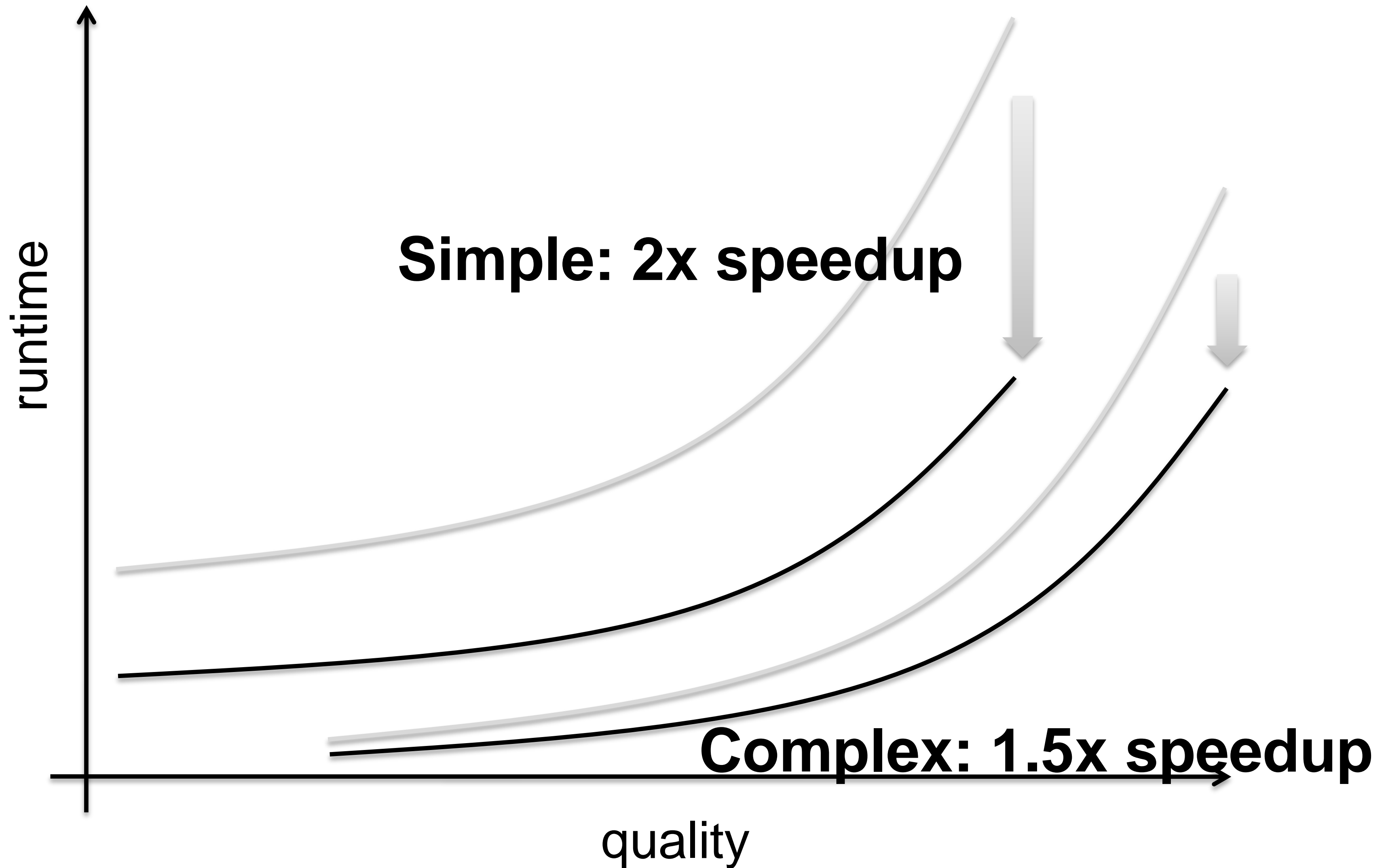
# So are we stuck with this?

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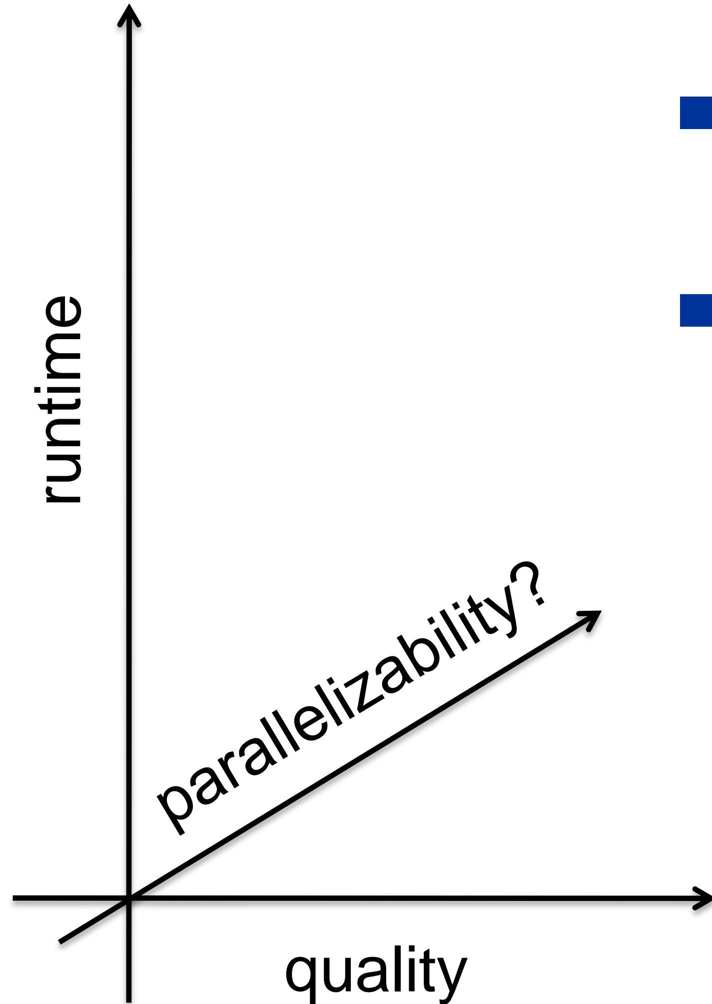
# Parallelizability: a third dimension?




- Not entirely independent of quality or runtime
- But there may be optimizations that don't have a large impact on quality or (serial) runtime

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# Example: Quartus II router

- Dynamically assigns nets to processors
  - A type of partitioning
- No loss of runtime or quality when run in serial

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# Example: Quartus II placement?

- Currently: we do not partition
  - Therefore, every move can interact with every other move
- Future work: *biased* moves
  - Cores would *tend* to work on cells in physical regions of the chip
  - Therefore moves *tend* not to interact
  - Can simplify interaction tracking/resolving in many cases
- Hopefully will improve parallelizability without otherwise impacting runtime or quality

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# Quality summary

- Be careful what algorithms you parallelize
- Be careful of simplifications that impact quality
- High-quality algorithms may be harder to parallelize for less speedup
  - But overall quality might still be better

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# Conclusions

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# Future work

- We continue to face three major challenges:
  - Development issues (eg tools, testing)
  - Ensuring determinism
  - Balancing parallel speedups with quality
- Good news: fascinating research opportunities
  - Also: parallel CAD software engineers remain gainfully employed
- Are you a parallel researcher?
  - You may find these topics interesting and useful to investigate
- Are you a tool vendor?
  - Maybe this gives you some ideas for future products

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# Thanks!

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