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Message from the Chair

As the third quarter of 2008 ensues, we look back to a half year of sustained level of activity at DATC. Our online newsletter includes unique summaries of emerging conferences around the world, "first-view" opinion in emerging and / or technology-market topics, and summaries of our own meetings and events. Our collaboration with our Society and Council remains strong, including helping our CEDA Council with a new worldwide chip design certification program and emerging online activities. Finally our web site keeps improving thanks to our Online Chair Joe Damora.

Please see more details below in our online newsletter, with instructions at the end if you want to submit contributions. We look forward to ending 2008 on a high note.

Future Shock - Semiconductors and Software

By *Gary Smith*

One of the more interesting consequences in the move to Electronic System Level design, has been the Semiconductor Industry's reaction to the challenge. Keep in mind we have been putting microprocessors into ASICs since the late 1980s so the software connection isn't new. What is new is that the responsibility for embedded design has shifted.

In 1998 we moved to the 180nm semiconductor node, which provided the engineer enough available gates, 35 million, to design true systems on a chip. These designs became known as SoCs. Bryan Lewis, of Gartner Dataquest defined a SoC as an ASIC including at least one processing element. Prior to that we had been designing chip-sets in which one of the chips contained the processor. The other ASICs completed the system.

The real change occurred in 2006. By that time Semiconductor vendors were supplying SoCs to the Chinese consumer OEMs that were selling into the US market. These Semiconductor vendors were also supplying demo kits that gave the manufacturer the board layout and just about everything else needed to complete the electronics for many of the consumer products; the main example was the MP3 player. That year John Barber, of Gartner Dataquest, reported that Wal-Mart had a return rate of 65% of the MP3 players that they had sold for Christmas. The culprit was a confusing user interface. The result was that the Chinese OEMs requested that the US semiconductor vendors supply the software needed to run the MP3 players. All of a sudden the Semiconductor world was being held responsible for the SoC's embedded software.

About the same time it became clear that in their search for a more power

friendly SoC architecture that the Semiconductor Industry had abandoned the high frequency Von Neumann computer architecture in favor of a slower multi-core architecture. What it took them a while to understand was that they had also abandoned the sequential Von Neumann Model of Computation, which had driven computer architecture from the late 1940s, to a multi-core computer architecture that had no Model of Computation. The initial response, from the semiconductor vendors was, "Not my job." Unfortunately that was also the response from the Software Industry. The Embedded vendors proclaimed that parallel computing had been tried, and failed, for over 25 years and that they didn't intend to waste R&D resources trying again. Microsoft claimed that a jury rigged version of C, F#, would work just fine. That's when the microprocessor vendors started getting worried.

2007 was another pivotal year. The ITRS, after much debate over whether software was part of their charter, took a look at the software issue. The result was that software was included in the ITRS Cost Chart, an auxiliary part of the roadmap. The results showed that developing the software for an SoC had passed the cost of designing the silicon during 2007. It also showed that unless we developed some type of concurrent software development infrastructure by 2012, that the cost of producing a SoC would have a negative impact on the continuation of Moore's Law's curve. That resulted in the inclusion of software in the main body of the roadmap for 2008.

Bottom line is that we are in trouble. We recognized the problem five years too late and then were slow getting into action. We have four years to come up with a concurrent infrastructure and we have yet to come up with a Model of Computation. There is a lot of questioning the resources being spent on turning C into a concurrent language. We are spending billions of dollars solving the back end lithography issues for IC manufacturing, we are spending billions of dollars designing SoCs, and we are spending millions of dollars on the concurrent software problem. Something has to change.

ICCAD and Designers...

By *Juan-Antonio Carballo*

ICCAD has recently previewed its Designers' Panels at www.iccad.com. Already past its 25th anniversary, the conference continues to evolve and grow. In 2008, ICCAD presents this mature program focused on designers' issues, at the core of its overall technical program. Two designers' sessions will be held. Both sessions will have Mondira Pant from Intel Corp. and Mar Hershenson from Magma Design Automation as moderators,

Challenges at 45nm and Beyond

Design at 45nm technologies and below is a risky proposition because of the many design challenges involved: variability, leakage, verification complexity, poor analog device performance, etc. In this panel, experienced designers coming from different backgrounds talk about how they have overcome some of the design and CAD challenges in 45nm, what CAD challenges still exist and how the CAD community can help.

This session will have the following outstanding speakers: Daniel W. Bailey, an AMD Fellow and Senior Design Manager for a team working on the physical design of a low-power x86 microprocessor; Eric Soenen, opened TSMC's new Austin Design Center, and created a new Power Management product line;

Puneet Gupta, a faculty member of the Electrical Engineering Department at UCLA; and Paul Villarrubia, technical lead for IBM's physical synthesis system.

Mixed-signal simulation challenges and solutions

The design of complex mixed-signal system-on-a-chip (SOC) designer poses challenging requirements on the simulation design environment. The simulation platform has to include simulations at the behavioral, gate and transistor-level which have traditionally been done in separate environments. As the scaling trend continues, the designer needs additional accuracy and capacity, new capabilities such as efficient statistical simulation that takes into account layout dependent effects. In this panel we have representatives from the CAD and design community discussing the challenges and current solutions available to the mixed-signal simulation challenge.

This outstanding session will feature equally outstanding speakers, including: Henry Chang, who co-founded Designer's Guide Consulting in 2005; William W. Walker, who is Vice President in charge of the Circuits and Devices Innovation Group at Fujitsu Laboratories of America; John Maneatis, TCI's co-founder, President, and Chief Technologist; John Croix, Founder and CTO of Nascentric.

Preview of Asia and South Pacific Design Automation Conference 2009

By *Kazutoshi Wakabayashi*

ASP-DAC 2009 is the fourteenth annual international conference on VLSI design automation in Asia and South Pacific region. It will be held in Yokohama, Japan, on January 19-22, 2009, jointly with the Electronic Design and Solution Fair 2009. The conference will provide the CAD/DA and Design community with opportunities of interchanging ideas and collaboratively discussing the directions of the technologies related to all of Electronic Design Automation (EDA).

The conference consists of keynote speeches, tutorials, the designers' forum, technical sessions, the university LSI design contest, and the IEICE VLD student forum. On the first day, one full-day and six half-day tutorials are scheduled, which will provide the audience with an introduction to hot topics in design for variability, reliable circuit design, low leakage design, multi-core software development, embedded system design, and functional verification. On the remaining three days, the technical program starts with keynote speeches:

- Mitsuo Saito, Chief Fellow and VP of Engineering, Toshiba Corporation Semiconductor Company: "Challenges to EDA System from the View Point of Processor Design and Technology Drivers"
- Neil Harry Earle Weste, Director, NHEW R&D Pty Ltd. and Blue Bay Helicopters Pty Ltd.: "Climate Change, Global Warming and IC Design (or How to survive as a dinosaur.)"
- Leon Stok, Director, Electronic Design Automation, IBM Systems and Technology Group, "From Restrictive to Prescriptive Design"

As for technical sessions, we received 355 submissions, and 116 papers were selected and compiled into an exciting final program which is further enriched by multiple special sessions. Designers' forum is a unique program which

consists of invited talks and panels to share design experience and solutions of real product designs of the industries. Its topics include up-to-date consumer SoCs, analog technologies, dynamic reconfigurable processors, and upstream design methods. For more information, please visit our website www.aspdac.com.

Preview of MSE 2009

By *Andrzej Rucinski*

The IEEE Computer Society International Conference on Microelectronic Systems Education is the premier conference dedicated to furthering undergraduate and graduate education in designing and building innovative microelectronics systems. The conference is held in the U.S. in odd years, and in Europe in even years, when it is called the European Workshop on Microelectronics Education (EWME). MSE is co-located with the Design Automation Conference (DAC).

The MSE conference provides an excellent opportunity for educators and industry to work together to ensure continued excellence in the field of microelectronic systems. Of particular interest is incorporation of trends in the microelectronic system industry and research into the classroom. This year's theme, "Educating System Designers in the Multi-core, Ubiquitous Computing Era," brings together current relevant topics including omni-present electronics in the form of cell phones, mp3 players, and even wearable computers with the emergence of chip multiprocessors for laptops and gaming consoles.

Papers are invited but not limited to the following areas:

- Education techniques including novel curricula and laboratories, distance learning, textbooks, and design projects.
- Industry and academic collaborative programs and teaching.
- Preparing students for industry, entrepreneurship, academics, and/or research.
- Educational infrastructure such as design and IP libraries and access to design tools.
- Novel education strategies for all MSE topics including but not limited to embedded processors, multi-processors, VLSI design, CAD, ASICs, ASIPs, DSP, and FPGAs.

Papers submitted to MSE 2009 should not exceed four (4) pages in length. Submissions must comply with IEEE Computer Society formatting requirements. Submissions may be submitted on-line at www.mseconference.org. Submissions will be judged on originality, appropriateness, technical strength, assessment, and other relevant criteria. Expanded versions of selected papers will be considered for inclusion in a special issue of IEEE Transactions on Education based on MSE 2009.

The MSE conference is collaborating with the SIGDA/DAC University Booth located on the Design Automation Conference floor, to schedule a special session on Microelectronics Systems Education on Monday, July 27, 2009 in the afternoon just following the official close of the conference. MSE participants are invited to conduct demonstrations of their projects during this special session and/or throughout the week during DAC. MSE contributors who wish to participate in this event are requested to register their demonstration at the University Booth website, www.sigda.org/ubooth.html.

Registration typically opens three months prior to the Design Automation Conference.

Call for Contributions On Multiprocessing for EDA

By *Dwight Hill and Juan-Antonio Carballo*

The IEEE DATC welcomes proposals for “crowd sourcing” contributions to address the overall problem of multiprocessing for EDA. In particular, we consider such problems as logic synthesis and/or routing on many processors. These problems can be divided across processors in several ways, but this tends to introduce an element of indeterminacy. For example, if one synthesizes each cone of logic independently and then re-assemble them, the result will depend on the relative machine speeds. This makes it very, very difficult to apply such parallel processing in practice, if for no other reason than it cannot be debugged. An approach that would mitigate this problem would be invaluable, especially if it were applicable to a broad range of EDA problems.

Contributions will be accepted until December 31, 2008, and should not exceed one page in length in the form of an essay. Up to three winners will be selected and published in DATC avenues, including this newsletter and invitation to provide a presentation at ICCAD’s annual meeting in San Jose in November 2009. Contributions should be sent to jantonio@ieee.org.

Contribution Opportunities

The IEEE DATC welcomes proposals for contributions to this newsletter. Contributions should shed light on non-obvious key EDA trends. Educational contributions in emerging areas such as ESL and DFM are especially welcome. The ideal length of a contribution is a half a page in the form of a short fact-based essay with data or references backing the stated position, but longer contributions may be considered. Publication of important graphics and data tables might be possible by request. Please send proposals in the form of a 2-paragraph abstract to the editors at jantonio@ieee.org.